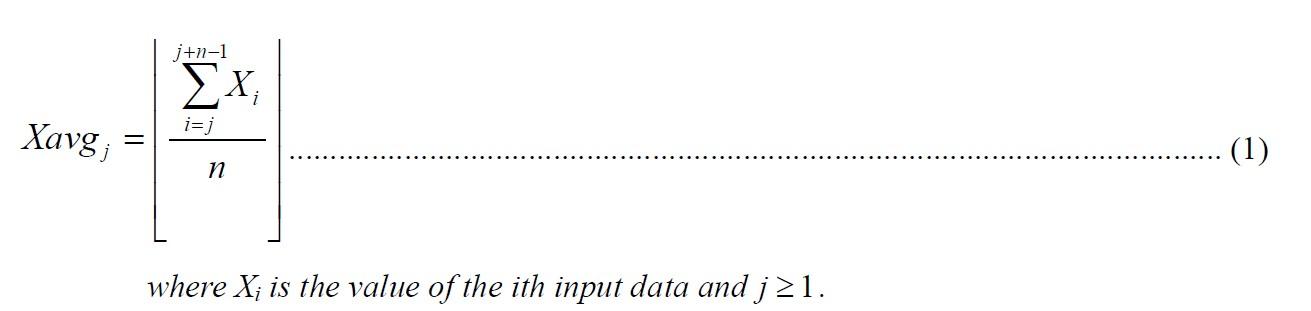
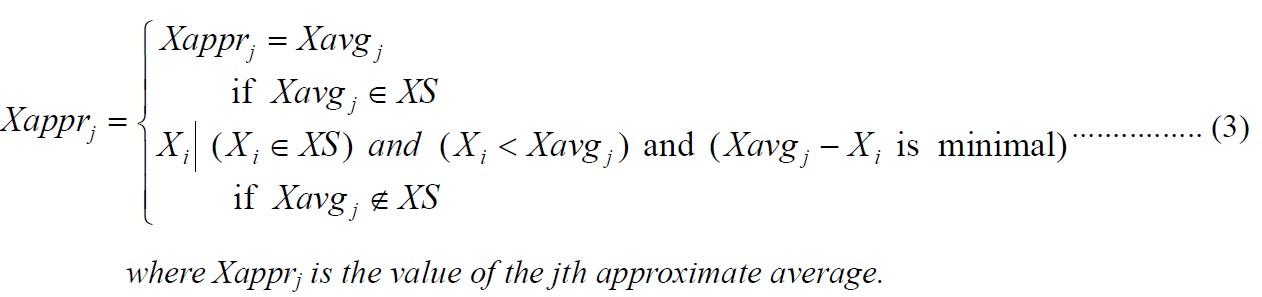
# Homework 1：Approximate Average (紹軒)

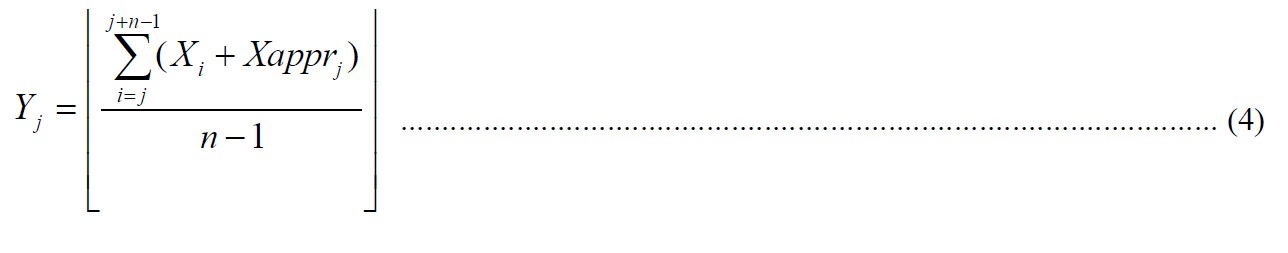
## 1.Introduction

Please design a computational system whose transfer function is defined as follows. A series of 8-bit positive integers is generated as the input of the computational system by the test bench. The output value Y is a 10-bit positive integer, which is calculated according to equations (1), (2), (3) and (4).









The computational system produces the output sequence according to the given input sequence. Each input and output data in the respective sequence is indexed. This index, in terms of hardware, is the relative time when the input data is given or the output data is ready. Thinking as a hardware designer, the approximate average is chosen from the last n input data which should be stored in the system. The system should be able to calculate the integral part of the real average of the last n input data first. And then if the integral part of the real average equals to any one of the last n input data, the approximate average is simply the integral part. Else the approximate average is the one which is one of the last n input data whose value is smaller than and closest to the integral part of the real average. The above descriptions stated the desired operations as those defined by equations (1), (2), and (3).

After the approximate average is obtained, the output value can be calculated according to equation (4). First, the last n input value is added by the corresponding approximate average. And then they are summed up and divided by n-1. The output value is the quotient after division.

For example, assume that n=4, X1=3, X2=24, X3=16, X4=8, and X5=3. After the first 5 input items are given, the system should store them and calculate the output value. The average of the first 4 input values is 12(only the integral part is left). Since it is not in the set of {X1, X2, X3, X4}, the system selects one from {X1, X2, X3, X4} as the approximate average whose value is smaller than 12 and close to 12. In this case, the approximate average is 8. So the first output value is calculated n as

⌊[(3 + 8) + (24 + 8) + (16 + 8) + (8 + 8)] / [(4 - 1)]⌋ = 27 .

Similar to those described above, when the 5th input data item is given, the system should store X2, X3, X4 and X5 and calculate the corresponding output value. The 2nd output value should be the same as the first one because the values stored in the system are the same.

## 2. General rules for deliverables

You need to complete this homework **INDIVIDUALLY**. You can discuss the homework with other

students, but you need to do the homework by yourself. You should **NOT copy** anything from

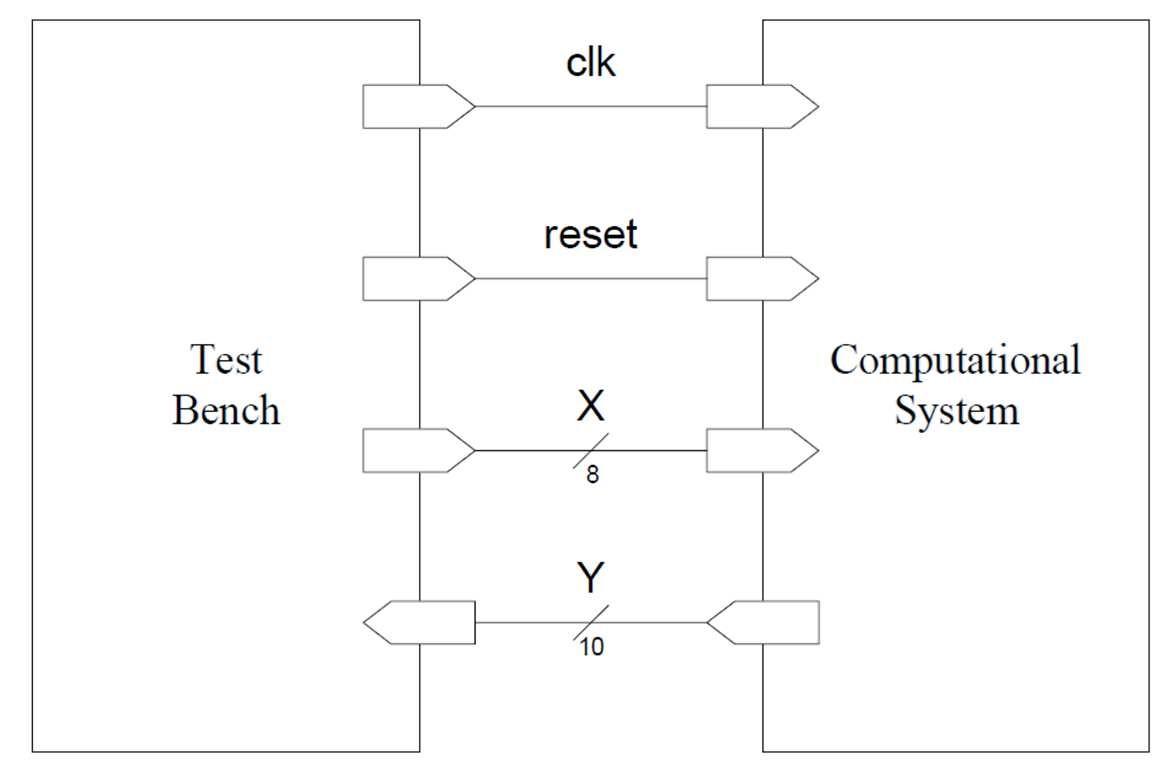
someone else, and you should **NOT distribute** your homework to someone else. If you violate any of

under these rules, you will get **NEGATIVE scores**, or even fail this course directly.

1. CS.v (Modify the code to pass TA's testbench, **We will use our own test data to test.** ).

## 3. Design Specifications

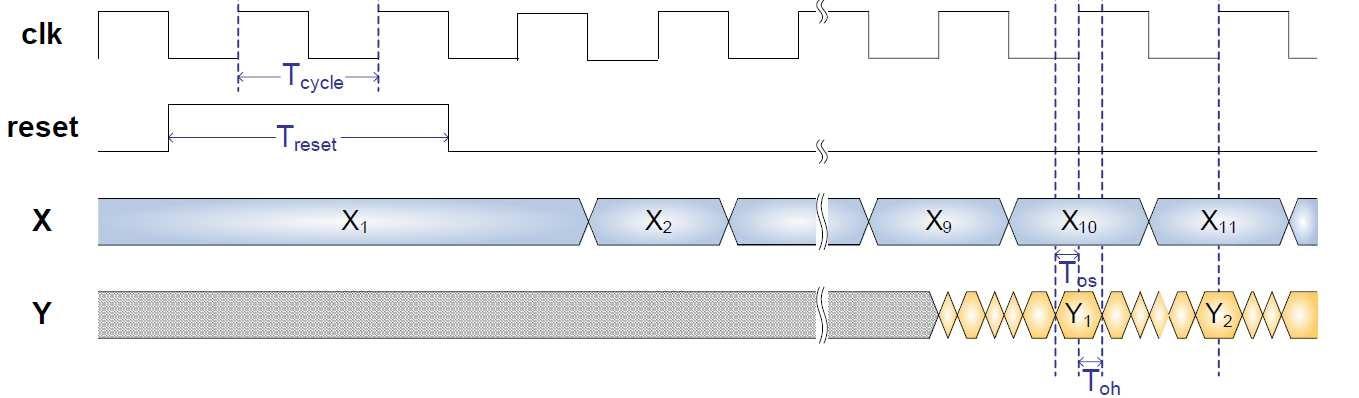
* Block Overview

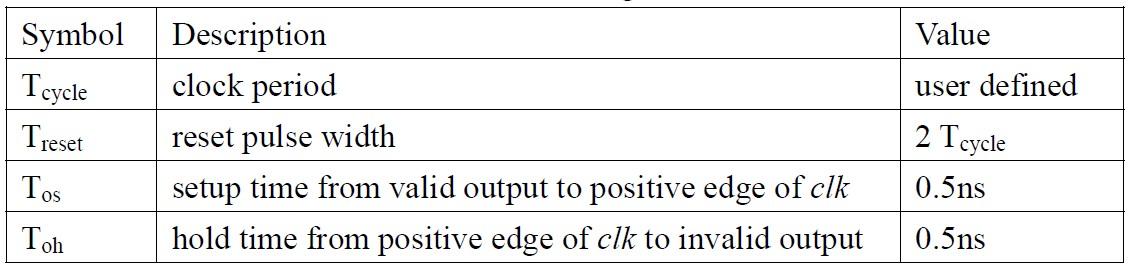


* I/O Interface

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | I/O | width | Description |
| clk | I | 1 | clock for the computational system |
| reset | I | 1 | reset the state of the computational system when it asserts |
| X | I | 8 | input data of the computational system |
| Y | O | 10 | computed output |

* Timing Diagrams



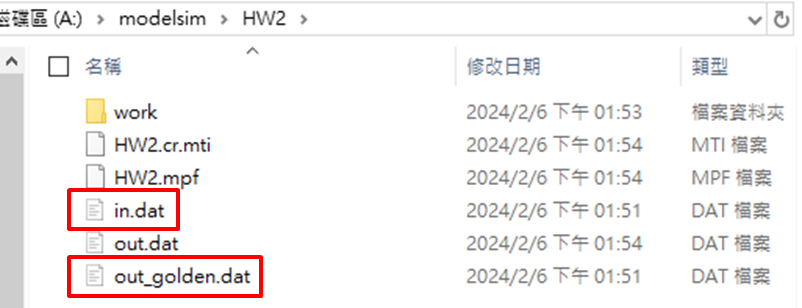


The I/O timing diagram is as shown above. For this homework, n in equations (1)(4) are fixed to 9. The computational system is reset by asserting a reset signal for 2 periods. The input X is changed to the next at the negative edges of the clock while output Y is checked by the test bench at positive edges of the clock. Note that the output should be stable around the positive edges of the clock. The setup and hold time requirements for the output are listed in Table. The first output data should be valid after the input data changes from 9th one to 10th and before the next positive clock edge. After that, the output should be changed to the next at the next positive clock edge and so on, that is to say, the test bench checks one output value per clock cycle.

## 4. 注意事項

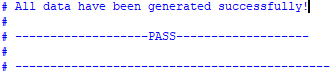
作業下載連結 : [HW2\_ApproxAvg](https://drive.google.com/drive/folders/1ZuWhqC_6j5y7-z84Z0ZRo4a9LpxZ59HF?usp=sharing)

記得要將in.dat和out\_golden.dat移入modelsim 的專案路徑之下，否則將會無法讀到in.dat和out\_golden.dat.

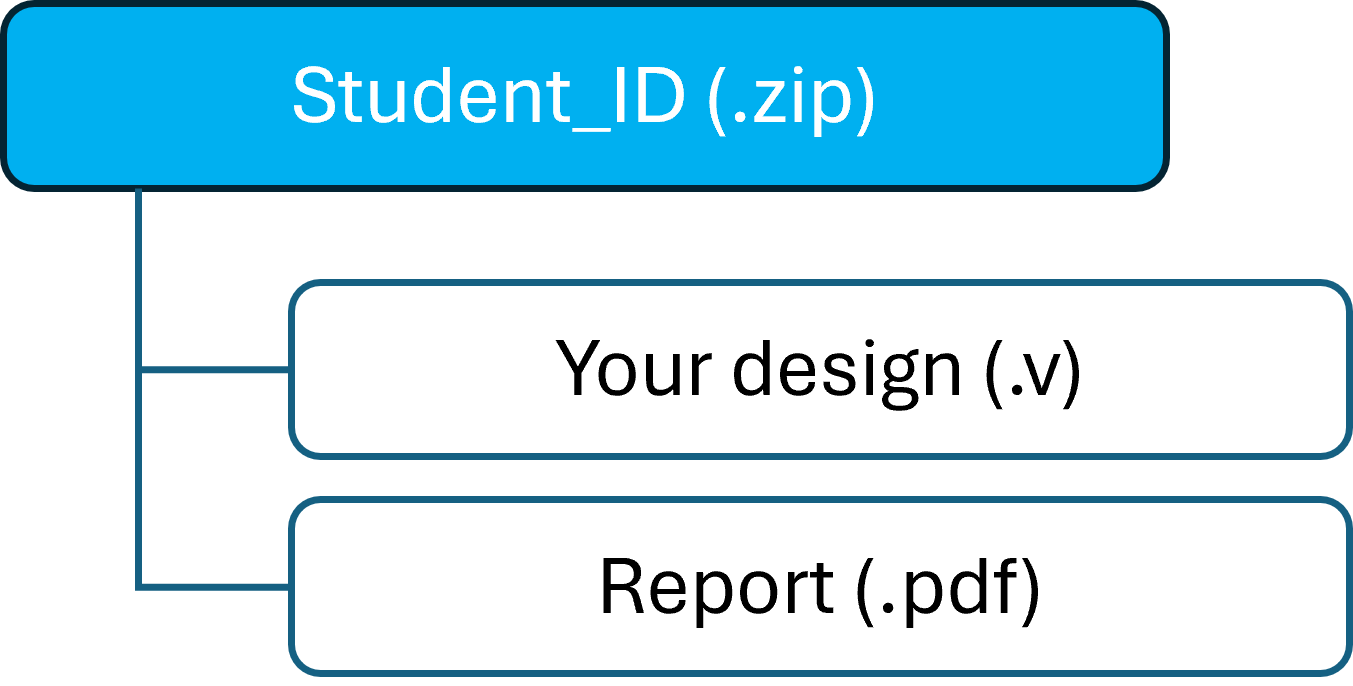


out.dat是會紀錄你的每一筆output，所以不用做移入或是刪除的動作。

## 5. Scoring

* **Pass modelsim simulation to get 80% (according to how many tests you pass.)**
  + **有出現下圖訊息即可。**
  + ****
* **Report document 20%**
  + **Architecture Diagram**
  + **Explain your design**
  + **Learn from this homework**

## 6. File Hierarchy



## 7. Appendix

